REMARKS

An Excess Claim Fee Payment Letter is submitted herewith for four excess claims.

Claims 1-24 are presently pending in this application. Claims 1-3, 5 and 7-11 have been amended to more particularly define the invention. Claims 12-24 have been added to assure Applicant the degree of protection to which his invention entitles him.

Claims 1, 3, and 4 were rejected under 35 U.S.C §102(b) as being anticipated by Nagano, U.S. Patent No. 5,687,003. Claim 2 was rejected under 35 U.S.C §103(a) as being unpatentable over Nagano, in view of Koji, Japanese Patent Publication No. 08-298601 or Murakami, Japanese Patent Publication No. 40-1176119A. Claims 5-6 were rejected under 35 U.S.C §103(a) as being unpatentable over Nagano, in view of Hasegawa, et al., U.S. Patent No. 5,384,645. Claims 7 and 9-11 were rejected under 35 U.S.C §103(a) as being unpatentable over Nagano and Hasegawa, in view of Nagai, U.S. Published Patent Application No. 2001/0010561. Claim 8 was rejected under 35 U.S.C §103(a) as being unpatentable over Nagano, Hasegawa, et al. and Nagai, in view of Kubo, et al., U.S. Patent No. 6,639,626. Claim 10 was rejected under 35 U.S.C §103(a) as being unpatentable over Nagano, Hasegawa, et al. and Nagai, in view of Yoshihiro, Japanese Patent Publication No. 11-261871. These rejections are respectfully traversed.

In an exemplary embodiment, the claimed invention is directed to an image sensing apparatus which includes an image quality mode setting block for setting only one of a plurality of image quality modes, a solid state image sensing element for converting an optical image into an analog electrical signal, and an analog-to-digital conversion block for converting the analog signal from the solid state image sensing element into a digital signal.

The analog-to-digital conversion block converts the analog signal into a digital signal which has a quantization bit count corresponding only to the image quality mode set by the image quality mode setting block.

Thus, even though the image quality mode setting block is able to set a plurality of image quality modes, and the analog-to-digital conversion block is able to provide a corresponding plurality of quantization bit counts, only one image quality mode is set, and only one quantization bit count is utilized. Consequently, accurate operation is assured.

Nagano discloses a reader with a high-resolution mode and a high-speed mode.

Koji shows a video signal processor in which level-compressed signals are converted into digital video signals with regulated word length. The levels of the video signals are compressed so that the rate of the resolution of digital video signals is held to a desired level.

Murakami shows a parallel analog-to-digital converter in which the resolution may be set with a switch at a node corresponding to the required resolution.

Hasegawa shows an image rotating apparatus which controls write/read addresses every B/N pieces on bringing together input image data having N-bit information per pixel in accordance with a word width B.

Nagai shows an image sensing apparatus and method including a video signal processing circuit which downsamples pixels is such a manner that the number of pixels constituting one frame of an image becomes the number of pixels on an image displayed on a display unit. The image data can be recorded on a memory card and displayed from that memory. The image sensing apparatus might be an electronic still camera.

Kubo shows a photographing apparatus with two image sensors of different sizes.

The apparatus includes interpolation units.

Yoshihiro shows an image pickup device in which when an image is displayed, power is supplied to the display circuitry and is cut to the image pickup element and the image processing components.

Applicant's independent claim 1 includes an image quality mode setting block for setting only one of a plurality of image quality modes, a solid state image sensing element, and an AD conversion block for converting the analog signal output from the solid state image sensing element into a digital signal with a quantization bit count corresponding only to the one image quality mode set by the image quality mode setting block.

As depicted in Nagano's Figure 1, Nagano's reader includes a CCD sensor 40 which converts an optical image into an analog electrical signal, a first analog-to-digital converter 51 with a high quantization bit count which provides a high-resolution output, a second analog-to-digital converter 42 with a low quantization bit count which provides a high-speed output, a data selector 53 which continuously receives the outputs of both AD converters 51 and 42, and a control circuit 52 which provides a "fine" signal to data selector 53, enabling the data selector to output either the high resolution output or the high speed output.

From Nagano's disclosure it is clear that both AD converters operate regardless of the mode desired. Thus, Figure 1 clearly shows that the "ADIN" input is continuously applied to both AD converter 51 and AD converter 42 and shows that the outputs from both converters are continuously applied to data selector 53. Further the "fine" control signal from control circuit 52 is applied only to data selector 53. There is nothing that controls the inputs, the operation, or the outputs of the two AD converters.

Further, at column 4, lines 58-62, Nagano states: "Also, to the output of the first AD convertor 51 and that of the second AD convertor 42, a data selector 53 for selecting an output from the first AD convertor or the second AD convertor 42 and for sending it out to the control circuit 52 is connected." (Emphasis added.) And at column 5, lines 30-31 Nagano states: "A 12-bit input A or input B [to data selector 53] is selected by the data selector 53."

Claim 1 thus distinguishes patentably from Nagano. The remaining references do not show that which distinguishes claim 1 from Nagano. Consequently, claim 1 is allowable, as are its dependent claims 2-12.

New independent claim 13 likewise distinguishes from the references in a patentable manner. Like claim 1, claim 13 includes an image quality mode setting block for setting only one of a plurality of image quality modes, and a solid state image sensing element. Claim 13 also includes an AD conversion block for converting the analog signal from the image sensing element into a digital signal. The AD conversion block has a plurality of quantization bit counts corresponding respectively to the plurality of image quality modes. The AD conversion block is responsive to the one image quality mode set by the image quality mode setting block to enable only the quantization bit count corresponding to the one set image quality mode, while disabling all other quantization bit counts. In the embodiment of Figure 1, the AD conversion block includes the AD converter 8 and the digital signal processing circuit 9. In the embodiment of Figure 5, the AD conversion block includes the three AD converters 20, 21, and 22, the switch 23, and the digital signal processing circuit 9. Consequently, only the one mode is active at any one time.

Dependent claims 12 and 13 add further features of Applicant's invention to claim 1 and are also allowable.

Independent claim 14 and its dependent claims 15-24 thus likewise distinguish patentably from the references.

The title has been amended to be more indicative of the invention to which the claims pertain and to overcome the Examiner's objection to the title.

The specification, drawings, and Abstract have been amended to correct minor errors and to assure grammatical and idiomatic English and improved form under United States practice.

In view of the foregoing, Applicant submits that claims 1-24, all the claims presently pending in the application, are patentably distinct over the prior art of record and that the application is in condition for allowance. Such action would be appreciated.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

To the extent necessary, Applicant petitions for an extension of time under 37 C.F.R. §1.136. Please charge any shortage in the fees due in connection with the filing of this paper,

including extension of time fees, to Attorney's Deposit Account No. 50-0481 and please credit any excess fees to such deposit account.

Respectfully Submitted,

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